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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/458,506	12/09/1999	TAE-GYOUNG KANG	5484-53	8916

7590 11/21/2001

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EXAMINER
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NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

DATE MAILED: 11/21/2001

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/458,506

Applicant(s)

Kang

Examiner

ORI NADAV

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on Oct 2, 2001.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-25 and 29-39 is/are pending in the application.
- 4a) Of the above, claim(s) 1-13 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 14-25 and 29-39 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

- 13) ☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).
- a) ☐ All b) ☐ Some\* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\*See the attached detailed Office action for a list of the certified copies not received.

- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

- 15) ☐ Notice of References Cited (PTO-892) 18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 19) ☐ Notice of Informal Patent Application (PTO-152)
- 17) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). \_\_\_\_\_ 20) ☐ Other:

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## **DETAILED ACTION**

### ***Specification***

1. The disclosure is objected to because of the following informalities: There is no "Brief Description" of figure 17.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 14-25 and 29-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Bothra et al. (6,020,616) and Japanese Patent (9-289251).  
  
APA teaches in figure 10 a substrate 1, active regions of two or more adjacent transistors having source and drain regions and at least one first and second electrodes having first and second metals connected to the source and drain regions to supply voltage thereto, a plurality of transistor gates on the substrate between the

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electrodes, wherein two or more gates are of a predetermined width and length at a substantially identical gap between ones of the adjacent transistor gates on the substrate.

APA does not teach a plurality of dummy gates having a predetermined width and length between ones of the transistors at a substantially identical gap between adjacent ones of the dummy gates as that between the adjacent ones of the transistor gates on the substrate.

Bothra et al. teach in figure 3L a plurality of dummy gates 226 having a predetermined width and length between ones of the transistors at a substantially identical gap between adjacent ones of the dummy gates, and being commonly connected on a substrate.

Japanese Patent (9-289251) teaches in figure 3 a plurality of dummy gates and transistor gates on the substrate having substantially identical gap between them, and being commonly connected to a first metal to supply a ground voltage.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a plurality of dummy gates having a predetermined width and length between ones of the transistors at a substantially identical gap therebetween, wherein the gap between adjacent ones of the dummy gates is substantially identical as that between the adjacent ones of the transistor gates in APA's device in order to reduce the inductive noise of the device (by providing a

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plurality of dummy gates having a predetermined width and length between ones of the transistors at a substantially identical gap therebetween) and in order to simplify the processing steps of making the device (by providing a substantially identical gap between adjacent ones of the dummy gates as that between the adjacent ones of the transistor gates), respectively.

Regarding claims 15, 19, 23 and 26, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the length of the dummy gates substantially the same as that of the transistor gates in order to simplify the processing steps of making the device.

Regarding claims 16, 20 and 24, APA teaches in figure 10 transistor gates having common terminals each of which connected on the substrate.

4. Claims 14-25 and 29-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Patent (9-289251).

Japanese Patent (9-289251) teaches in figures 1 and 5 a substrate 1, active regions of two or more adjacent transistors having source and drain regions (figure 9) and at least one first and second electrodes having first and second metals connected to the source and drain regions to supply voltage thereto, a plurality of transistor gates PS1-PS3 on

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the substrate between the electrodes, wherein two or more gates are of a predetermined width and length at a substantially identical gap between ones of the adjacent transistor gates on the substrate, and a plurality of dummy gates 1a, 2a, 1b, 2b, being commonly connected to a first metal to supply a ground voltage, and having a predetermined width and length between ones of the transistors at a substantially identical gap between adjacent ones of the dummy gates as that between the adjacent ones of the transistor gates on the substrate.

The claimed limitations of 'adjacent transistor gates and adjacent dummy gates' do not require the transistor gates and the dummy gates to be located next to each other, respectively, without intervening dummy gates and transistor gates, respectively, therebetween. Note that the broadest meaning of the term 'adjacent' is defined as 'nearby'. Therefore, the gap between PS1 and PS3 (figure 1) is substantially identical to the gap between two adjacent dummy electrodes (figure 5, section 1). Thus, the claimed structure is considered to be at least obvious over the structure of Japanese Patent (9-289251).

Regarding claims 15, 19, 23 and 26, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the length of the dummy gates substantially the same as that of the transistor gates in order to simplify the processing steps of making the device.

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***Response to Arguments***

5. Applicant's arguments with respect to claims 14-25 and 29-39 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

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Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772**.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav

November 11, 2001

Steven Loke  
Primary Examiner

